



Serial No. 09/526,814
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REMARKS

The Final Office Action mailed August 20, 2002, has been received and reviewed. Claims 1 through 4 and 15 through 25 are currently pending in the application. Claims 1 through 4, and 15 through 25 stand rejected. Applicant proposes to amend claims 1, 15 and 17, and respectfully requests reconsideration of the application as proposed to be amended herein.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,436,503 to Kunitomo et al.

Claims 1 through 4, 15 through 17, and 19 through 25 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Kunitomo et al., U.S. Patent No. 5,436,503. Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claims 1 through 4

Independent claim 1 of the presently claimed invention, as proposed to be amended herein, is directed to an apparatus for routing interconnections among bond pads on a semiconductor die. The apparatus includes a sheet-like, non-conductive structure having a first surface and a second surface for attachment to a semiconductor die. A plurality of electrically conductive discrete pads are attached to the first surface of the sheet-like, nonconductive structure. The plurality of electrically conductive discrete pads each include an electrical connect portion and *an electrically isolated portion comprising a portion facing said first surface and a periphery defined thereabout.*

The Examiner cites Kunitomo, with specific reference to FIG. 3, as disclosing a semiconductor device comprising a sheet-like, nonconductive structure (11) having a first surface and a second surface for attachment to the semiconductor die; a plurality of electrical conductive discrete pads (12) attached to the first surface, the plurality of electrically conductive discrete pads each having an electrical connection portion facing the first surface, each electrically isolated about the portion facing the first surface. However, Applicant submits that Kunitomo fails to disclose a plurality of electrically conductive discrete pads having *an electrically isolated portion comprising a portion facing said first surface and a periphery defined thereabout*.

Kunitomo is directed to a flip chip-type semiconductor device (also referred to by Kunitomo as a "flip-flop" mounted device). The semiconductor device includes a semiconductor chip (10) having a plurality of bumped electrodes (9) on a surface thereof. The electrodes (9) of the semiconductor chip (10) are coupled with electrodes (12) of an insulating substrate (11). The insulating substrate is "composed of a ceramic serving as a multi-layer circuit board" (col. 6, lines 22-23, emphasis added) and includes a plurality of external terminals 15 on an undersurface thereof for mounting and electrically coupling with a circuit board. (See, generally col. 6, lines 18-58).

It is clear from the description set forth in Kunitomo that the contact pads or electrodes (12) on the first surface of insulating substrate (11) are electrically coupled through the "multi-layered circuit board" to the external terminals 15 on the underside of the substrate 11. Such a configuration, therefore, includes a plurality of contact pads which clearly do not include an *electrically isolated portion comprising a portion facing said first surface and a periphery defined thereabout* as they are inherently electrically coupled to the layers of internally located circuitry formed in the insulating substrate 11 (i.e., the circuit board). Such is in contradistinction to claim 1 of the presently claimed invention wherein each of the conductive discrete pads include electrically isolated portions facing the first surface of the sheet-like nonconductive structure.

Applicant, therefore, respectfully submits that claim 1 is clearly allowable over Kunitomo. Applicant further submits that claims 2 through 4 are allowable as being dependent from an allowable base claim as well as for the additional patentable subject matter introduced thereby.

With respect to claim 2, the Examiner points to FIG. 3 of Kunitomo as disclosing the subject matter set forth therein. However, Applicants submit that Kunitomo fails to teach the plurality of discrete pads in their recited configuration, as noted above, and further fails to teach at least one conductor extending between at least two of such pads, wherein the at least one conductor includes at least a portion which is external to the sheet-like nonconductive structure.

Applicant, therefore, respectfully requests reconsideration and allowance of claims 1 through 4.

Claims 15, 16 and 19 through 21

Independent claim 15, as proposed to be amended herein, is directed to a semiconductor device having a die, including a plurality of conductive pads disposed on a surface thereof; an adapter having a first plurality of discrete electrical contacts on a first surface thereof with each being electrically connected to one of the plurality of bond pads, and a second plurality of discrete electrical contacts on a second surface thereof, each of said second plurality of discrete electrical contacts having an electrical connection portion and *an electrically isolated portion comprising a die facing portion and a periphery defined thereabout*, at least some of the second plurality of discrete electrical contacts being in electrical communication with the first plurality of discrete electrical contacts; and a plurality of conductive bumps, each extending from one of the second plurality of discrete electrical contacts.

Applicant submits that Kunitomo fails to teach a plurality of discrete electrical contacts having an electrical connection portion and an electrically isolated die facing portion. Rather, as set forth above, Kunitomo teaches a semiconductor device having a semiconductor die (10) electrically coupled with an insulating substrate (11). The insulating substrate includes a

plurality of contacts or electrodes (12) which are then electrically interconnected with a plurality of external terminals (15) on an underside thereof by way of a "multi-layer circuit board" comprising the substrate (11). Clearly, from the description given by Kunitomo, the electrodes (12) do not include an electrically isolated portion comprising a die facing portion and a periphery defined thereabout. As such, Applicant submits that claim 15 is clearly allowable over Kunitomo.

Additionally, Applicant submits that claims 16 and 19 through 21 are allowable as being dependent from an allowable base claim as well as for the additional patentable subject matter introduced thereby.

With respect to claim 19, Applicant submits that Kunitomo fails to teach at least one conductive via extending between at least one of the first plurality of discrete electrical contacts and at least one of the at least some other of said second plurality of discrete electrical contacts. Rather, as noted above, Kunitomo indicates that the insulating substrate is formed as a multi-layer circuit board suggesting to one of ordinary skill in the art that electrical connections between the electrodes (12) and external terminals (15) comprise one or more layers of circuit traces or similar circuitry.

With respect to claim 20, Kunitomo fails to teach a discrete electrical contact on the adapter which is electrically isolated from the plurality of bond pads disposed on the first surface of the die. While the Examiner cites FIG. 3 as disclosing such subject matter, Applicant fails to see the disclosure of such subject matter therein. Moreover, Applicant submits that FIG. 3 may not be relied upon for determining if one of the external terminals (15) is electrically isolated from the plurality of electrodes (12) or vice versa as no specific circuitry is shown which would indicate such isolation.

Applicant, therefore, respectfully requests reconsideration and allowance of claims 15, 16 and 19 through 21.

Claims 17 and 22 through 25

Independent claim 17 is directed to a semiconductor device. The semiconductor device includes a die having a plurality of bond pads disposed on a first surface thereof; and an adapter having a first plurality of discrete electrical contacts on a first surface thereof, each being electrically connected to one of said plurality of bond pads, and a second plurality of discrete electrical contacts on a second surface thereof, at least some of said second plurality of discrete electrical contacts being horizontally remote from at least some of the plurality of bond pads disposed on the first surface of the die, *the at least some of said second plurality of discrete electrical contacts having an electrically isolated portion comprising a die facing portion and a periphery defined thereabout*, and at least some other of said second plurality of discrete electrical contacts being electrically connected to said first plurality of discrete electrical contacts.

Applicant submits that Kunitomo fails to teach that *at least some of said second plurality of discrete electrical contacts have an electrically isolated portion comprising a die facing portion and a periphery defined thereabout*. Rather, as set forth above, Kunitomo teaches a semiconductor device having a semiconductor die (10) electrically coupled with an insulating substrate (11). The insulating substrate includes a plurality of contacts or electrodes (12) which are then electrically interconnected with a plurality of external terminals (15) on an underside thereof by way of a "multi-layer circuit board" comprising the substrate (11). Clearly, from the description given by Kunitomo, the electrodes (12) do not include an electrically isolate portion comprising a die facing portion and a periphery defined thereabout. As such, Applicant submits that claim 17 is clearly allowable over Kunitomo.

Applicant further submits that claims 22 through 25 are allowable as being dependent from an allowable base claim, as well as for the additional patentable subject matter introduced thereby.

With respect to claim 23, Kunitomo fails to teach plurality of conductive vias extending through the adapter electrically connecting the first plurality of discrete electrical contacts and the at least some other of the second plurality of discrete electrical contacts. Rather, as noted above, Kunitomo indicates that the insulating substrate is formed as a multi-layer circuit board suggesting to one of ordinary skill in the art that electrical connections between the electrodes (12) and external terminals (15) comprise one or more layers of circuit traces or similar circuitry.

With respect to claim 25, Kunitomo fails to teach that at least one of the second plurality of discrete electrical contacts is electrically interconnected with a second die.

Applicant, therefore, respectfully requests reconsideration and allowance of claims 17 and 22 through 25.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,436,503 to Kunitomo et al. and further in view of U.S. Patent No. 4,712,129 to Orcutt

Claim 18 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kunitomo et al.(U.S. Patent No. 5,436,503) as applied to claim 15 above, and further in view of Orcutt (U.S. Patent No. 4,712,129). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 18 is improper because the references relied upon fail to teach or suggest all the limitations of the presently claimed invention.

Claim 18 of the presently claimed invention depends from claim 17. Claim 18 recites that the adapter set forth in claim 17 further comprises a material having a coefficient of thermal expansion substantially matching the coefficient of thermal expansion of the die. The Examiner relies on Kunitomo as teaching all the limitations of claim 17, and then cites Orcutt as teaching "that the texture and the die have similar TCE in order to prevent cracking between the die and the substrate." (Office Action, page 3). Further, the Examiner states that "it would have been obvious of one of ordinary skill in the art at the time of the invention was made to use the matching TCE of Orcutt's in Kunitomo et al. in order to prevent the cracking between the die and the substrate." (Office Action, page 4).

As addressed above with respect to claim 17, Kunitomo fails to teach or suggest all of the limitations of claim 17. Particularly, Kunitomo fails to teach or suggest an adapter which includes *at least some of a second plurality of discrete electrical contacts having an electrically isolated portion comprising a die facing portion and a periphery defined thereabout*. Orcutt likewise fails to teach or suggest such subject matter. Thus, the combination of Kunitomo and Orcutt fail to teach or suggest all of the limitations of the presently claimed invention as set forth in claim 18.

Applicant, therefore, submits that claim 18 is allowable over Kunitomo and Orcutt, taken either individually or in combination, and respectfully request reconsideration and allowance thereof.



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ENTRY OF AMENDMENTS

The proposed amendments to claims 1, 15 and 17 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, Applicants submit that the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1 through 4 and 15 through 25 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully Submitted,

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Date: October 18, 2002

BBJ/kla:djp

Enclosure: Version with Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Three Times Amended) An apparatus for routing interconnections among bond pads on a semiconductor die, comprising:
a sheet-like, nonconductive structure having a first surface, and a second surface for attachment to said semiconductor die; and
a plurality of electrically conductive discrete pads attached to said first surface, the plurality of electrically conductive discrete pads each having an electrical connect portion and [a] an electrically isolated portion comprising a portion facing said first surface and a periphery defined thereabout], each electrically conductive discrete pad of the plurality being electrically isolated about said portion facing said first surface].

15. (Twice Amended) A semiconductor device, comprising:
a die including a plurality of bond pads disposed on a surface thereof;
an adapter having a first plurality of discrete electrical contacts on a first surface thereof, each electrically connected to one of said plurality of bond pads, and a second plurality of discrete electrical contacts on a second surface thereof, each of said second plurality of discrete electrical contacts having an electrical connection portion and [a] an electrically isolated portion comprising a die facing portion and [each being electrically isolated about said die facing portions] a periphery defined thereabout, at least some of said second plurality of discrete electrical contacts in electrical communication with said first plurality of discrete electrical contacts; and
a plurality of conductive bumps, each extending from one of said second plurality of discrete electrical contacts.

17. (Twice Amended) A semiconductor device, comprising:
a die including a plurality of bond pads disposed on a first surface thereof;
an adapter having a first plurality of discrete electrical contacts on a first surface thereof, each electrically connected to one of said plurality of bond pads, and a second plurality of discrete electrical contacts on a second surface thereof, at least some of said second plurality of discrete electrical contacts being horizontally remote from at least some of the plurality of bond pads disposed on the first surface of the die, the at least some of said second plurality of discrete electrical contacts [being electrically isolated about a] having an electrically isolated portion comprising a die facing portion and a periphery defined thereabout [thereof], and at least some other of said second plurality of discrete electrical contacts being electrically connected to said first plurality of discrete electrical contacts.